UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/622,734	11/27/2000	Keisuke Koga	YAO-432US	2803

7590 10/29/2003

Andrew L Ney
Ratner & Prestia
Suite 301 One Westlakes Berwyn
PO Box 980
Valley Forge, PA 19482-0980

EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/622,734	KOGA, KEISUKE
	Examiner	Art Unit
	Johannes P Mondt	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,7,9-14 and 17-22* is/are allowed.

6)☒ Claim(s) *4-6,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Amendment filed 08/04/2003 forms the basis of this office action. In said Amendment of 08/04/2003 Applicant amended claims 1, 4 and 5, cancelled claim 8, while claims 1-7 and 9-22 are pending. Comments on Remarks in said Amendment are included below under "Response to Arguments".

Response to Arguments

1. Applicant's arguments filed 08/04/2003 have been fully considered but they are partly persuasive, but to an important degree not persuasive. To wit:

Grounds for Double Patenting have disappeared with the cancellation of claim 8.

The present claim 1 is patentable over Kuriyama in view of Kojima. Kojima specifically teaches that "the source region to be symmetrical in structure with its associated drain region" (column 12, lines 19-27). Motivation to include the teaching by Kojima in the invention by Kuriyama is provided by the analogue of the intermediate gate electrode 105 (column 9, line 4) in the form of extraction electrode 2: reduction of the influence of the capacitance between said extraction electrode 2 in Kuriyama, - corresponding to the intermediate gate electrode 105 in Kojima, and the corresponding drain 103 is the primary motivation (see column 12, lines 19-27). However, it does not necessarily follow from the above that within the drain region itself both wells must have *"impurity concentrations having symmetrical impurity distributions", because the symmetry taught literally by*

Kojima is confined to inter-source-drain symmetry, not intra-drain symmetry. The rejection of claim 1 and dependent claims is therefore withdrawn. After an update of the search, taking into account the broader language of the currently amended claim 1, claims 1-3 and 14 (dependent upon claim 1) are herewith indicated as allowed.

However, claim 4 is rejected as before, because the gate electrode 8 is clearly provided such as to cover an end of the drain region (cf. Figure 3; where it is evident that said gate electrode partially covers region 4, which is part of the drain region by virtue of being contiguously connected with drain region 6. Although this feature is in evidence in cited material including Figure 3, the office action will be non-final for not having particularly spelled out this feature.

Furthermore, claim 5 is again rejected, because the gate 8 is buried in the first insulation film in Kuriyama the gate insulation film, i.e., the film between the gate and the substrate 5, is thinner than the first insulating film. The reason for this is the lower voltage to which the gate electrode is exposed (cf. column 5, lines 4-11 and also Figure 3, as cited before).

Because traverse of claim 6 appears to be only based on the alleged shortcomings of the rejection of claim 5, the rejection of claim 6 is herewith also repeated.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claims 4 and 15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5,550,435) in view of Kojima (5,965,921) and Kawaguchi (JP401061953A) (as listed in the Information Disclosure Statement of Paper No. 5).

With regard to claim 4: Kuriyama et al teach (cf. Figure 3) a field emission type electron source device (cf. title and abstract) comprising:

a field emission electron source portion including an extraction electrode 2 (cf. column 4, line 38) provided on a p-type silicon substrate 5 (cf. column 4, line 39) via an insulating film 3 (cf. column 4, line 38) and having an opening portion (located around 1, see Figure 3) at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion (comprising IGFET gate 8, channel between source 6 and drain 4/6; cf. column 4, line 41) provided on the p-

type silicon substrate, corresponding to the field emission electron source portion, wherein:

the field emission electron source portion is provided in a drain region 4/6 (cf. column 4, lines 39-40) of the field effect transistor portion; and a control voltage is applied to a gate electrode 8 (cf. column 4, line 41) of the field effect transistor portion to control a field emission current from the field emission source portion., while the aforementioned gate electrode 8 is positioned lower than the extraction electrode 2.

Kuriyama et al do not necessarily teach the further limitation that the gate electrode of the field effect transistor portion has a shape such that a portion of the gate electrode nearer the drain region has a total width wider than a total width of a portion of near the source region. However, in order to prevent hot carrier generation in a depletion layer of the drain junction, Kawaguchi teaches a gate electrode 1 in a MOS transistor to be wider on the drain side 2 than on the source side 3 (see "Purpose" and "Constitution" in Abstract).

Motivation to include the teaching of Kawaguchi in this regard in the invention by Kuriyama et al stems from the circumstance that suppression of said hot carrier generation would increase the withstand voltage in any MOSFET, irregardless of whether said MOSFET is incorporated into a field emission cathode apparatus of the type essentially taught by Kuriyama et al, while an attempt to achieve an overall increase the withstand voltage is in line with the objective of Kuriyama et al (see column 1, line 55 – column 2, line 11).

Furthermore, all that is necessary for a *combination* of the inventions is a widening of the gate near the drain. Therefore, *reasonable expectation of success* is justified.

The extraction electrode as taught by Kuriyama et al is provided in a region above the drain region and away from an interface between regions of different impurity concentrations, namely the region in the upper right corner of Figure 3 marked "Grid Electrode").

4. ***Claims 5 and 16*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5,550,435) in view of Kojima (5,965,921). Kuriyama et al teach (cf. Figure 3) a field emission type electron source device (cf. title and abstract) comprising:

a field emission electron source portion including an extraction electrode 2 (cf. column 4, line 38) provided on a p-type silicon substrate 5 (cf. column 4, line 39) via an insulating film 3 (cf. column 4, line 38) and having an opening portion (located around 1, see Figure 3) at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode 2; and

an n-channel field effect transistor portion (comprising IGFET gate electrode 8, channel between source 6 and drain 4/6; cf. column 4, line 41) provided on the p-type silicon substrate, corresponding to the field emission electron source portion, wherein:

the field emission electron source portion is provided in a drain region 4/6 (cf. column 4, lines 39-40) of the field effect transistor portion; and a control voltage is applied to a gate electrode 8 (cf. column 4, line 41) of the field effect transistor portion to control a field emission current from the field emission source portion;

the drain region includes at least two wells 4 and 6 having different impurity concentrations (4 is n-doped and 6 is n+ doped silicon) (cf. column 4, lines 45-46); and

of the at least two wells, one well having a low impurity concentration is provided at an end of the drain (said drain being to the left of the channel between drain and source; cf, Figure 3) which contacts the channel region of the field effect transistor portion.

Kuriyama et al do not necessarily teach the further limitation that the well having low impurity concentration is provided around a circumference of the other well having a higher impurity concentration. However, as is evidenced by Kojima, it is well known in the art of field effect transistors with insulated gate that the rated voltage can be improved by surrounding the heavily doped drain region by a lightly doped drain region so as to further reduce the gate-drain capacitance; see column 9, lines 1-40 and column 11, line 54 – column 12, line 8). The relevant component in Kuriyama is indeed a field effect transistor with insulated gate, and hence the art is analogous.

Motivation to include the teaching by Kojima in this regard is the desirability to improve the rated voltage for any insulated gate field effect transistor, including the

IGFET in the invention by Kuriyama et al. The inventions can be easily combined through slightly extending the lightly doped drain region. Success in implementing the combination of the teaching by Kojima and the invention by Kuriyama et al can therefore be reasonably expected.

The gate insulation film between the p-silicon substrate 5 and IGFET gate 8 as taught by Kuriyama et al is thinner than the first insulating film 3 (see Figure 3) while the first insulating film is provided between the extraction electrode 2 and the p-type silicon substrate 5, while the gate insulating film is buried with the first insulating film. Thus, it is concluded that claim 5 is unpatentable over Kuriyama et al in view of Kojima.

With regard to claim 16: the extraction electrode 2 as taught by Kuriyama et al is provided in a region above the drain region and away from an interface between regions of different impurity concentrations, namely the region in the upper right corner of Figure 3 marked "Grid Electrode". Therefore, the further limitations as defined by claims 14 and 16 do not distinguish over the primary reference (Kuriyama et al).

1. ***Claim 6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al and Kojima as applied to claim 5 above, and further in view of Hirano et al (JP409063467A).

As detailed above, Kuriyama et al anticipate Claim 5; however, they do not necessarily teach the further limitation of Claim 6. Nevertheless, it would have been obvious to use thermal oxidation to produce the insulating film as it is understood in the

art that silicon dioxide is an excellent insulating film generally in semiconductor field effect device technology while it is economically produced, given the silicon substrate suitable to provide the fuel, while *Hirano et al teach the use of thermal oxidation of silicon* for the more specific purpose of sharpening the tip of the cathode portion of the field emission electrode source portion of their cold cathode device; see [0034] and title and abstract. *Motivation* to combine stems from the requirement of a micropoint of the electron emitter taught by Kuriyama et al; see their claim 1 for instance. *Combinability* of the inventions by Kuriyama et al and Hirano et al is obvious in view of the efficiency of producing said tip and gate insulating film together in this manner. *Reasonable expectation of success* of the combination of said inventions follows from the fact that no new steps are introduced at any stage.

Allowable Subject Matter

5. ***Claims 1-3 and 14*** are allowed. The following is a statement of reasons for the indication of allowable subject matter:

> Kojima specifically teaches that "the source region to be symmetrical in structure with its associated drain region" (column 12, lines 19-27). Motivation to include the teaching by Kojima in the invention by Kuriyama is provided by the analogue of the intermediate gate electrode 105 (column 9, line 4) in the form of extraction electrode 2: reduction of the influence of the capacitance between said extraction electrode 2 in Kuriyama, - corresponding to the intermediate gate electrode 105 in Kojima, and the corresponding drain 103 is the primary

motivation (see column 12, lines 19-27). However, it does not necessarily follow from the above that within the drain region itself both wells must have *"impurity concentrations having symmetrical impurity distributions", because the symmetry taught literally by Kojima is confined to inter-source-drain symmetry, not intra-drain symmetry.* The rejection of claim 1 and dependent claims is therefore withdrawn. After an update of the search, taking into account the broader language of the currently amended claim 1, claims 1-3 and 14 (dependent upon claim 1) are herewith indicated as allowed.

2. ***Claims 7 and 17*** are allowable.

3. The following is a statement of reasons for the indication of allowable subject matter: Shielding electrodes in the art of field emission type electron sources with field effect transistor and made of the same material as the gate electrode, are known in the prior art as witnessed by *Ishikawa et al (JP60124872).* However, although this teaching would be pertinent to the MOSFET aspect of the invention by Kuriyama et al, said shielding electrode by Ishikawa et al (a) is not held at the same potential as the substrate, and (b) is neither shown nor described to cover a region of the channel. Shielding electrodes with the additional two features (a) and (b) described above have not been found in the Prior Art to date, nor has any reason surfaced as to why such shielding electrodes should be obvious.

4. ***Claims 9-13 and 18-22*** are allowed. The following is a statement of reasons for the indication of allowable subject matter: Although the first portion of claim 9 is taught by Kuriyama, i.e., up to and including line 14 on page 67 of the claim as printed in the disclosure, Kuriyama et al do not teach the further limitation for the drain region (lines 15-18), nor the further limitation for the gate electrode (lines 19-22), the latter with the exception that the gate electrode 8 is positioned lower than the extraction electrode 2, which is taught by Kuriyama et al (see discussion of claim 1). Although Shimomura et al is valid art under 102(a) unless the earliest of the two foreign priority documents is perfected, and although Shimomura et al teach within the context of a MOSFET that the drain 2 should be surrounded by the source region 3 (Figure 1 and page 9, Embodiment 1), and although the teaching by Shimomura et al further includes a symmetrical placement of the gate with respect to the *drain*, both teachings being motivated by the reduction of electric noise through fluctuations particularly for high-frequency applications (cf. abstract and page 6, line 57 – page 7, line 19 and page 8, lines 5-19), no teaching of a similar nature with regard to a symmetrical placement of the gate with respect to the emission cathode in a field effect device is available. The same comment applies to claim 18, which is taught by Kuriyama et al up to and including line 14 on page 5 of Amendment C, while, with the exception of the teaching by Kuriyama et al of the positioning of the gate electrode at a location lower than the extraction electrode, the further limitations on the drain region of the field effect transistor portion and on the gate electrode of the field effect transistor portion are identical to those in claim 9, and

hence the same comment applies to the close but incomplete teaching by Shimomura et al in this regard.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
October 22, 2003